LAW OFFICES
BARRY R. LIPSITZ
BRADFORD GREEN, BUILDING 8
755 MAIN STREET
MONROE, CONNECTICUT 06468

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BARRY R. LIPSITZ
RALPH F. HOPPIN
DOUGLAS M. McALLISTER

TELEPHONE: (203)459-0200
FACSIMILE: (203)459-0201

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

UTILITY PATENT APPLICATION TRANSMITTAL
FILED UNDER 37 C.F.R. §1.53(b)

Sir:

Transmitted herewith for filing is the patent application of:

Inventor(s): **Brian JOSEPH**

Title: **STORAGE EFFICIENT MINIMIZATION LOGIC**

APPLICATION ELEMENTS:

(1) [X] Patent Application Specification, including Abstract and claims - 19 pages
(2) [X] Three (3) sheets of formal drawings, together with transmittal letter
(3) [X] A check in the amount of $469.00 to cover the [X] filing fee ($429.00) and/or [X] Assignment Recordal Fee ($40) is enclosed.

[ ] Before calculating the fee, cancel claim(s)
[ ] Before calculating the fee, see copy of Preliminary Amendment filed in parent application _____ (attached hereto.)

Basic Fee								$	345.00
Multiple Dependent Claims ($260.)									
Foreign Language Surcharge ($130.)									
	For	No. Filed	-	No. Extra		Rate			
EXTRA	Total Claims	25	20	5	x	$ 9.	=	$	45.00
CLAIMS	Independent Claims	4	3	1	x	$39.	=	$	39.00
						TOTAL FILING FEE	=	$	429.00

[X] The Commissioner is hereby authorized to charge any deficiency in the payment of the required fee(s) or credit any overpayment to Deposit Account No. 50-0625.

(4) [X] Declaration and Power of Attorney form -- 3 pages
- a. [X] Newly executed
- b. [ ] Copy from a prior application
- c. [ ] Deletion of inventor(s) – signed statement attached deleting inventor(s) named in the prior application.

(5) [X] Small Entity Declaration
- a. [X] Newly executed
- b. [ ] Copy from a prior application. Status still proper and desired.

ACCOMPANYING APPLICATION PARTS:

(6) [X] Assignment document
- a. [X] Newly executed (with $40.00 recordal fee) and separate transmittal Form PTO-1595
- b. [ ] Copy from a prior application

(7) [ ] Preliminary Amendment

(8) [ ] Certified Copy of Priority Document, together with separate transmittal letter

(9) [ ] Information Disclosure Statement, together with PTO Form 1449 and copies of cited references

(10) [X] Return receipt postage prepaid postcard

(11) [X] Express Mail Certificate (Mailing Label No. EL 430 852 229 US)

(12) [ ] Other:
- a. [ ]

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(13) [ ] If a **CONTINUING APPLICATION,** check appropriate box, and supply the requisite information below:

☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)
of prior application no.:
Prior application information:
Examiner: _____ Group/Art Unit:_____
Status: _____

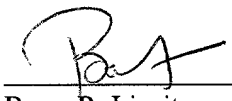
FOR CONTINUATION or DIVISIONAL APPLICATIONS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under paragraph 4(b) above, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

(14) [ ] Please amend the specification by inserting before the first line the sentence:

(15) [ ] This application claims the benefit of _____ Patent Application No. _____ filed on _____ .

(16) [**X**] Correspondence address:
Barry R. Lipsitz
Law Offices of Barry R. Lipsitz
755 Main Street, Building 8
Monroe, CT 06468
Telephone: (203) 459-0200

Respectfully submitted,



Barry R. Lipsitz
Attorney for Applicant(s)
Registration No. 28,637
755 Main Street
Monroe, CT 06468
(203) 459-0200

ATTORNEY DOCKET NO.: ALA-106
Date: March 21, 2000

03-22-00

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Brian JOSEPH

Application No.:

Filed: Herewith

For: **STORAGE EFFICIENT MINIMIZATION LOGIC**

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

EXPRESS MAIL CERTIFICATE

"Express Mail" mailing label number: **EL 430 852 229 US**
Date of Deposit: **March 21, 2000**

I hereby certify that the attached:

[x] Check in the amount of $469.00 (Filing fee ($429) and recordal fee ($40));
[x] Return receipt postage prepaid postcard;
[x] Transmittal letter for new patent application;
[x] Patent Application Specification, including Abstract and Claims (19 pages);
[x] Three (3) sheets of formal drawings, together with transmittal letter;
[x] Declaration and Power of Attorney form;
[x] Assignment, together with Form PTO-1595;
[x] Small Entity Declaration.

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: **BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231**

Myrna Hanff
(Typed or printed name of person mailing paper or fee)

Myrna Hanff
(Signature of person mailing paper or fee)

Respectfully submitted,

Date: **March 21, 2000**
ATTORNEY DOCKET NO.: **ALA-106**

Barry R. Lipsitz
Attorney for Applicant(s)
Registration No. 28,637
755 Main Street
Monroe, CT 06468
(203) 459-0200

Applicant or Patentee: **Brian JOSEPH**
Application or Patent No.:
Filed or Issued: **Herewith**
For: **STORAGE EFFICIENT MINIMIZATION LOGIC**

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 C.F.R. 1.9(f) and 1.27(c)) SMALL BUSINESS CONCERN

I hereby declare that I am
[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: **ALANTRO COMMUNICATIONS, INC.**
ADDRESS OF CONCERN: **141 Stony Circle, Suite 210**
Santa Rosa, California 95401

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 C.F.R. 121.3-18, and reproduced in 37 C.F.R. 1.9(d), for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled: **STORAGE EFFICIENT MINIMIZATION LOGIC**
by inventor(s) **Brian JOSEPH** described in [**X**] the specification filed herewith; [ ] application no. _____ filed _____ [ ] patent no. _____ issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 C.F.R. 1.9(d) or by any concern which would not qualify as a small business concern under 37 C.F.R. 1.9(d) or a nonprofit organization under 37 C.F.R. 1.9(e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 C.F.R. 1.27)

FULL NAME_____

ADDRESS_____

[ ] individual [ ] small business concern [ ] nonprofit organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 C.F.R. 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: **Eric J. Rossin**
TITLE OF PERSON OTHER THAN OWNER: **President**
ADDRESS OF PERSON SIGNING: **141 Stony Circle, Suite 210, Santa Rosa, California 95401**

SIGNATURE Eric J. Rossin

DATE 2/29/00

STORAGE EFFICIENT MINIMIZATION LOGIC

BACKGROUND OF THE INVENTION

The present invention relates to data processing techniques for use in communications systems and the like, and more particularly to the optimization of binary tree search structures used in such systems.

Determination of a minimum or maximum value in a set of data is a common operation which is often accomplished using specialized hardware. As an example, many communications systems utilize the Viterbi algorithm, which requires a determination of the most probable path for each state. This must be estimated by finding the path having the maximum metric (if correlation metric is used) or minimum metric (if Euclidean distance is used) among other concurrent paths. An efficient means for determination of the maximum or minimum metric is required.

A method for finding the minimum in an array of N values which is storage efficient is to store the running estimate of the minimum and its location and compare it to each of the $(N-1)$ other values in the array. This method requires $(N-1)$ comparisons which will take at least $(N-1)$ clock cycles.

For delay sensitive systems or for systems having fewer than (N-1) clock cycles to do the comparisons, a standard alternate approach is the binary tree search structure. In a binary tree search structure, each layer contains half as many comparators and storage elements as the previous layer, thus reducing the latency to $\log_2 N$ clock cycles and allowing for pipelining. The downside of such a structure is the addition of (N-1) comparators and storage elements.

For the foregoing reasons, there is a need for a method and apparatus which limits the latency inherent in systems using a running estimate and which reduces the number of storage elements used in a standard binary tree search structure.

SUMMARY OF THE INVENTION

The present invention is directed at a method and apparatus for considerably reducing the storage needed in a binary tree search structure.

In a preferred embodiment, an array of values is searched to find the minimum using a binary tree search structure in a storage efficient manner. A plurality of decision units are grouped in a plurality of computation stages. The number of decision units in a computation stage at level i is equal to $N/2^i$, N being the size of the array. Each computation stage reduces by ½ the set of values likely to contain the minimum of the array. Each decision unit in a computation stage takes as its input a pair of data values plus partial addresses of each data value, stores the minimum of the two values and adds to its partial address one most significant bit indicating the local address of the selected data value within the pair of inputs. In this embodiment, each computation stage adds one more bit of address until the entire address is known.

In one embodiment of the present invention, a system for locating a specific value contained in an array of N data values is used. The specific value is the result of a binary operation defined over the array of N data values wherein each data value is W bits wide. The system comprises a plurality of decision units grouped in

successive computation stages wherein each decision unit receives a pair of input values, each input value containing a data value and a partial address, and generates a value representative of a selected data value and the partial address of the selected data value. In this embodiment, the decision unit of the last computation stage contains the specific value.

In another embodiment, the present invention is related to an apparatus for obtaining information on a specific value within a pair of inputs, wherein each input contains a data value and a partial address of the data value, the apparatus comprising a binary operator which compares the data values and which generates as output a binary decision representative of a local address of the specific data value and a multiplexer which generates as output the specific data value along with its partial address based on the binary decision.

In yet another embodiment the present invention provides, in an array of N data values, a method of determining an address for a result. The result is the output of a binary operation defined in the array of data values, each data value having W bits. The method comprises the steps of performing, at each computation stage i of $\log_2 N$ computation stages, $N/2^i$ binary operations on the data values of $N/2^i$ pairs of input values. In this manner, each of the binary operations generates a binary decision representative of a local

address of a selected data value within the pair of input values and multiplexes, at each computation stage, each pair of input values to produce an output determined by the binary decision.

It is an object of the present invention to provide a method for finding a specific value in an array of data values, the method comprising the steps of grouping a plurality of decision units in a plurality of computation stages wherein the number of decision units in a computation stage at level i is equal to $N/2^i$, N being the size of the array, and processing the data values in each decision unit. A decision unit at a last computation stage determines the specific value.

The present invention can be used in any array having a transitive binary operator defined on it wherein the binary operator maps any pair to the Boolean set of {true, false}.

These and other features and objects of the invention will be more fully understood from the following detailed description of the preferred embodiments which should be read in light of the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of the specification, illustrate the embodiments of the present invention and, together with the description, serve to explain the principles of the invention.

Figure 1 shows a logic circuit for performing the method of the present invention;

Figure 2 shows the result obtained by applying the method of the present invention;

Figure 3 shows memory savings obtained with respect to previous techniques when using the present method and apparatus.

DETAILED DESCRIPTION OF THE INVENTION

In describing a preferred embodiment of the invention illustrated in the drawings, specific terminology will be used for the sake of clarity. However, the invention is not intended to be limited to the specific terms so selected, and it is to be understood that each specific term includes all technical equivalents which operate in a similar manner to accomplish a similar purpose.

With reference to the drawings in general and Figures 1 through 3 in particular, the apparatus of the present invention is disclosed.

Figure 1 shows a logic circuit for performing the method of the present invention, and illustrates a circuit for obtaining the minimum value contained in an array of data values along with its location address. In this embodiment, sixteen data values X15, X14,...,X0 contained in a memory area are searched to find the minimum value. Four computation stages, each having at least one decision unit, are used to determine the minimum and its location. Each computation stage prunes the number of possible values by one-half. In this embodiment, the possible values are the reduced set obtained from the array of data values by pruning half the values that are not the minimum values. The number

of decision units at each stage is equal to one-half the number of input values.

In this embodiment, each decision unit in a computation stage takes as its input a pair of data values plus partial addresses of each data value, stores the minimum of the two input values and adds to its partial address one most significant bit indicating which of the two data values was picked. Each computation stage adds one more bit of address until the address is completely known.

As illustrated in Figure 1, a decision unit is composed of a binary operator represented here as comparator 101, a multiplexer 103 and a storage element 105. Each comparator 101 at computation stage 100 takes as its input a pair of data values each eight bits long and outputs a binary decision representing the local address of the minimum data value within the pair. As an example, if X15 is the minimum compared to X14, the binary decision will be a binary 1 since "1" is the local address of X15 and "0" is the local address of X14 within the pair.

A multiplexer 103 at first computation stage 100 takes as its input a pair of values from the array of data values and outputs the input value selected by the binary decision. In this embodiment, the binary decision designates which input value corresponds to the Boolean "true" of the binary operator, and thus to the minimum of

the two input values. A storage element 105 at first computation stage 100 stores the output of its associated multiplexer 103.

In one embodiment, the storage element 105 stores the selected data value in one section of memory storage and adds a local address bit represented by the binary decision as its most significant bit to the partial address of the selected data value. Alternatively, the local address can be added as the least significant bit of storage element 105 and the selected data value can be the eight most significant bits.

In this embodiment, at first computation stage 100, the partial addresses of the data values are 0 bits wide. At first computation stage 100, each storage element 105 contains a selected data value and one bit representing the partial address of the selected data value. The set of data values contained in all storage elements of first computation stage 100 represents the reduced set of data values which are likely to contain the minimum of the array of data values. The minimum value of the array of data values is also referred to as a specific value according to the binary operation defined over the array of data values.

At second computation stage 110, each multiplexer 113 takes as its input the content of a pair of storage elements 105 of first computation stage 100. As an example, the inputs of multiplexer 113a are the content

of storage element 105a and 105b. In a preferred embodiment, the inputs of a decision unit are the two consecutive storage elements' contents of the previous computation stage. The inputs of the multiplexer 113 are each nine bits wide and represent an eight bit wide selected value plus one bit of partial address. In a preferred embodiment, the comparator 111 compares only the eight least significant bits of the input values to determine the minimum and outputs a binary decision. Storage element 115 stores the output of multiplexer 113 selected by the binary decision and adds the binary decision as the most significant bit to the partial address. At second computation stage 110, the possible values are reduced to a set of four elements.

The operation previously described in accordance with first computation stage 100 and second computation stage 110 is performed at each subsequent computation stage. At third computation stage 120, the decision units' inputs are ten bits wide while at fourth computation stage 130 they are eleven bits wide. The last stage, represented by fourth computation stage 130, contains only one decision unit, as illustrated in Figure 1. The storage element 135 contains four bits representing the entire address of the specific value which is stored in the eight least significant bits portion of the storage element 135.

Figure 2 illustrates the result obtained by applying the method of the present invention to an array of values. At each computation stage, the content of the storage elements is shown. The last computation stage contains the minimum value which is equal to one and its entire address which in binary format is 0101.

Although Figure 1 shows an array of values of size sixteen, the present invention can be applied to any array of values having a size N wherein N is a power of two and each value is W bits wide. The number of computation stages in this case is equal to $\log_2 N$. Each computation stage at level i, with $1 \leq i \leq \log_2 N$, contains $N/2^i$ decision units and each decision unit takes two inputs, each $(W+i-1)$-bit wide.

The method of the present invention can also be applied to any set which has a binary operation defined on it and wherein the binary operation has a transitive property. In particular, the method can also be used to find a maximum in an array of values.

The curve of Figure 3 shows the number of storage elements saved over the prior art when using the method and apparatus of the present invention. In the prior art binary tree search structure, the values along with their entire address are stored at each stage of the search, whereas with the present method only partial addresses are stored. The number of bit storage elements (NUM FLOPS) needed in the prior system is represented by the

following formula: $W(N-1)+\log_2 N(N-1)$. The number of bit storage elements needed for the present system is equal to $W(N-1)+2N-\log_2 N-2$. The overall storage savings can then be predicted by the formula: $N\log_2 N-2N+2$ which is represented by the curve of Figure 3.

Although the invention has been illustrated by reference to specific embodiments, it will be apparent to those skilled in the art that various adaptations and modifications may be made which clearly fall within the scope of the invention. The invention is intended to be protected broadly within the spirit and scope of the appended claims.

What is claimed is:

1. A system for locating a specific value contained in an array of *N* data values, the specific value being the result of a binary operation defined over the array of *N* data values wherein each data value is *W* bits wide, the system comprising a plurality of decision units grouped in successive computation stages wherein:
   (a) each decision unit receives a pair of input values, each input value containing a data value and a partial address; and
   (b) each decision unit generates a value representative of a selected data value and the partial address of the selected data value and the decision unit of the last computation stage contains the specific value.

2. The system of claim 1 wherein each of the plurality of decision units comprises:
   (a) a binary operator for generating a binary decision representative of a local address of the selected data value; and
   (b) a multiplexer for generating one of the pair of input values as output and with the output being selected by the binary decision.

3. The system of claim 2 wherein the binary operator selects the minimum value of the pair of data values contained in the pair of input values.

4. The system of claim 2 wherein the binary operator selects the maximum value of the pair of data values contained in the pair of input values.

5. The system of claim 1 wherein each of the plurality of decision units further comprises:

   (c) a storage element for storing the output of a multiplexer and the binary decision which is added to the partial address of the selected data value.

6. The system of claim 5 wherein the partial address of an input value at computation stage i is the $(i-1)$ most significant bit of the storage element of computation stage $(i-1)$.

7. The system of claim 5 wherein the partial address of an input value at computation stage i is the $(i-1)$ least significant bit of the storage element of computation stage $(i-1)$.

8. The system of claim 1 wherein the number of computation stages K is related to the size N of the array of data values by the formula $K = \log_2 N$.

9. The system of claim 8 wherein the number of decision units at a computation stage i is equal to $N/2^i$ and wherein $1 \leq i \leq K$.

10. The system of claim 8 wherein the last computation stage contains the address of the specific value in the K most significant bits of its associated storage element and the specific value is contained in the W least significant bits of said associated storage element.

11. The system of claim 8 wherein the last computation stage contains the address of the specific value in the K least significant bits of its associated storage element and the specific value is contained in the W most significant bits of said associated storage element.

12. An apparatus for obtaining information on a specific value within a pair of inputs, wherein each input contains a data value and a partial address of the data value, the apparatus comprising:
    (a) a binary operator which compares the data values and which generates as output a binary decision representative of a local address of the specific data value; and
    (b) a multiplexer which generates as output the specific data value along with its partial address based on the binary decision.

13. The apparatus of claim 12 further comprising:

(c) a storage element which stores the output of the multiplexer and the binary decision.

14. The apparatus of claim 12 wherein the binary operator is a minimum operator.

15. The apparatus of claim 12 wherein the binary operator is a maximum operator.

16. In an array of N data values, a method of determining an address for a result, the result being the output of a binary operation defined in the array of data values each data value having W bits, the method comprising the steps of:

(a) performing, at each computation stage i of $\log_2 N$ computation stages, $N/2^i$ binary operations on the data values of $N/2^i$ pairs of input values wherein each of the binary operations generates a binary decision representative of a local address of a selected data value within the pair of input values; and

(b) multiplexing at each computation stage each pair of input values and producing an output determined by the binary decision.

17. The method of claim 16 further comprising the step of

(c) storing at each computation stage the binary decision and the selected input in a storage element.

18. The method of claim 16 wherein the computation stage at level $\log_2 N$ contains the value of the result of the binary operation and its address within the array of values.

19. The method of claim 16 wherein the binary operation is a minimum finding operation.

20. The method of claim 16 wherein the binary operation is a maximum finding operation.

21. A method for finding a specific value in an array of data values, the method comprising the steps of:

(a) grouping a plurality of decision units in a plurality of computation stages wherein the number of decision units in a computation stage at level i is equal to $N/2^i$, N being the size of the array; and

(b) processing the data values in each decision unit;

wherein a decision unit at a last computation stage determines the specific value.

22. The method of claim 21 wherein each decision unit receives a pair of input values and generates as output a selected data value.

23. The method of claim 22 wherein the selected data value is the result of a binary operation performed on the pair of input values.

24. The method of claim 23 wherein the binary operation is a minimum finding operation.

25. The method of claim 23 wherein the binary operation is a maximum finding operation.

ABSTRACT OF THE DISCLOSURE

A system is provided for finding the result of a binary operation performed on an array of values, along with its address, in a storage-efficient manner. The system is based on a binary tree structure having a pipeline of binary operators and corresponding multiplexers and storage elements to store the outputs of the multiplexers in addition to the partial addresses of the outputs represented by the outputs of the binary operators. Each computation stage adds one more bit of address until the address is completely known at the last computation stage. The invention reduces the amount of storage required for keeping track of the addresses that are the result of the binary operation.

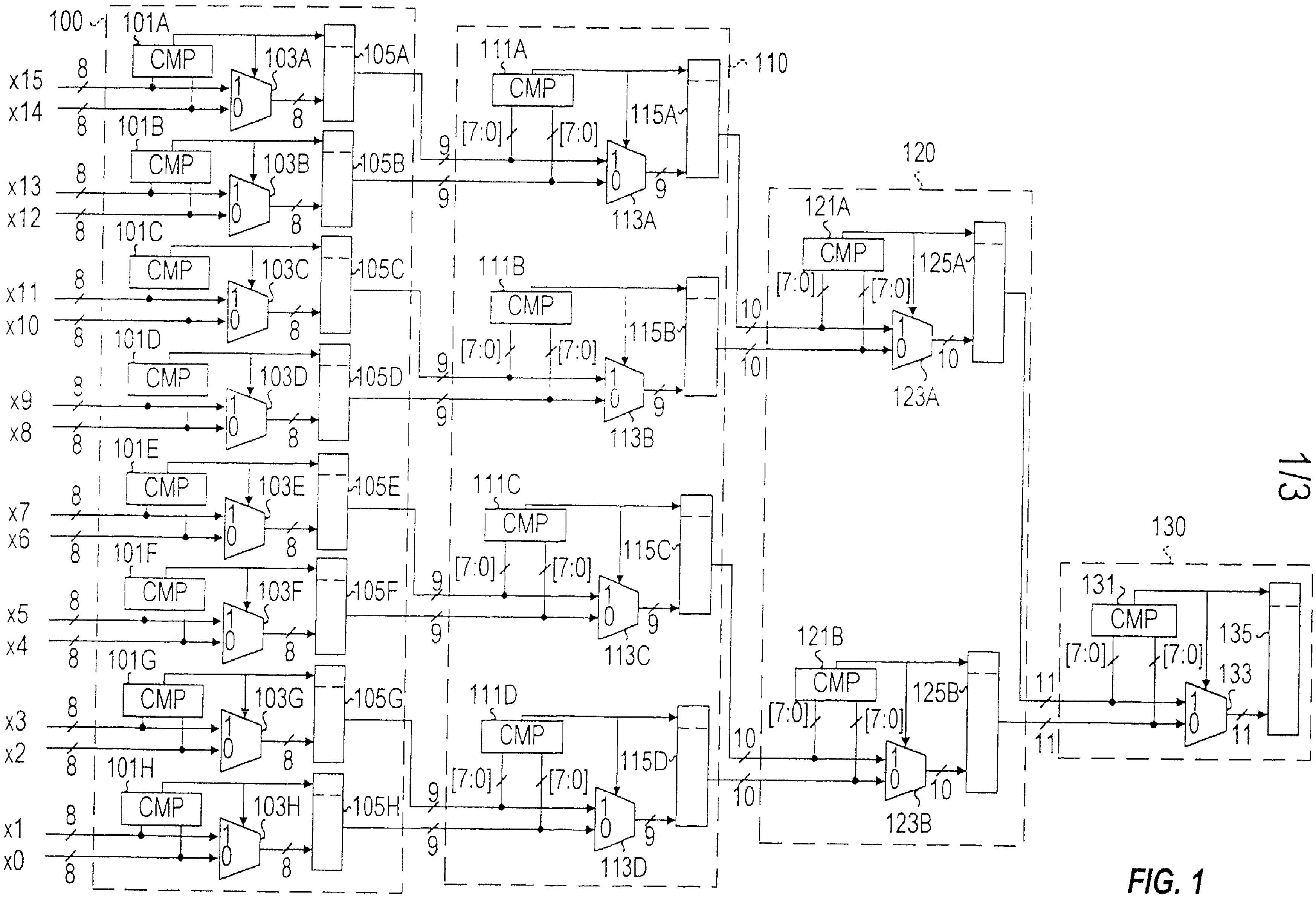

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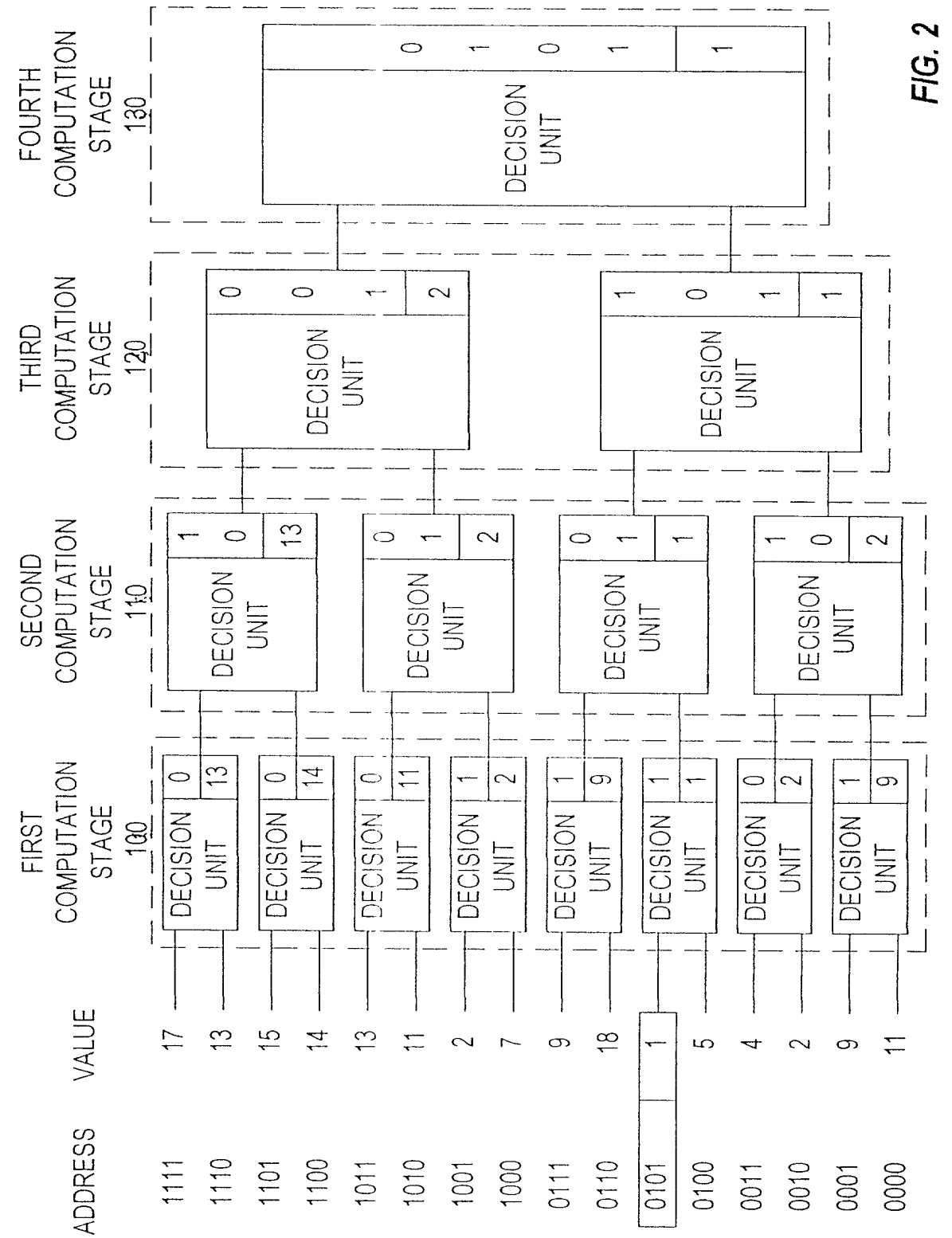
FIG. 1


FIRST COMPUTATION STAGE 100
SECOND COMPUTATION STAGE 110
THIRD COMPUTATION STAGE 120
FOURTH COMPUTATION STAGE 130
DECISION UNIT
ADDRESS
VALUE
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1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000
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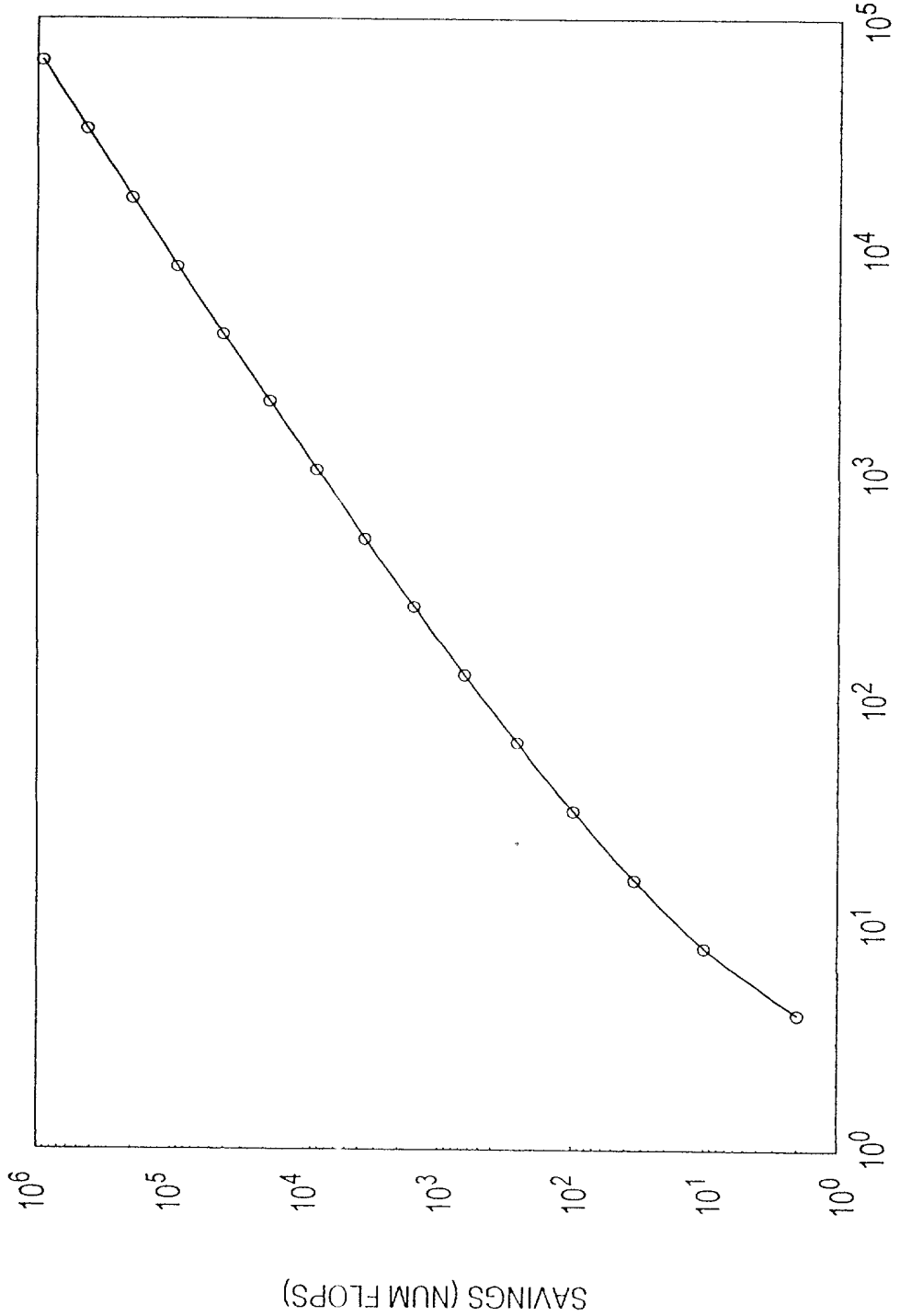
FIG. 2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10^1
10^2
10^3
10^4
10^5
10^6
10^0
10^1
10^2
10^3
10^4
10^5
SIZE OF INPUT ARRAY

FIG. 3

DECLARATION, POWER OF ATTORNEY, AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

STORAGE EFFICIENT MINIMIZATION LOGIC

the specification of which is attached hereto unless the following box is checked:

[ ] was filed on _____ as United States Application Number _____ or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed:

			Priority Claimed	
(Number)	(Country)	Month/Day/Year Filed	Yes	No
_____			[ ]	[ ]
(Number)	(Country)	Month/Day/Year Filed	Yes	No
_____			[ ]	[ ]

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date) - Month/Day/Year
_____	_____

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	**Parent Filing Date (MM/DD/YYYY)**	**Parent Patent Number (if applicable)**

And I hereby appoint: Barry R. Lipsitz, Registration No. 28,637, Ralph F. Hoppin, Registration No. 38,494 and Douglas M. McAllister, Registration No. 37,886, all of the firm of Barry R. Lipsitz, Attorney at Law, 755 Main Street, Bldg. 8, Monroe, Connecticut 06468, Telephone (203) 459-0200, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Brian JOSEPH

Inventor's Signature _____ Date: 02/29/2000

Residence **Tiburon** **California** Citizenship: **U.S.A.**
(City) (State or Foreign Country)

Post Office Address **40 Harbor Oak Drive, Apt. 25** **Tiburon, California 94920**
(Post Office Address) (City) (State & Zip Code/Country)